P2 Digital Electronics

Lecture 8: Digital to Analogue and Analogue to Digital Conversion

Mark Cannon
mark.cannon@eng.ox.ac.uk

Trinity Term 2026

Overview of lectures

1. Logical functions and logic gates
2. Low level logic design
3. Binary number representation
4. Binary arithmetic
5. Integration of digital logic components
6. Memory and sequential circuits
7. Design of sequential logic
8. **Data converters: analogue to digital / digital to analogue**

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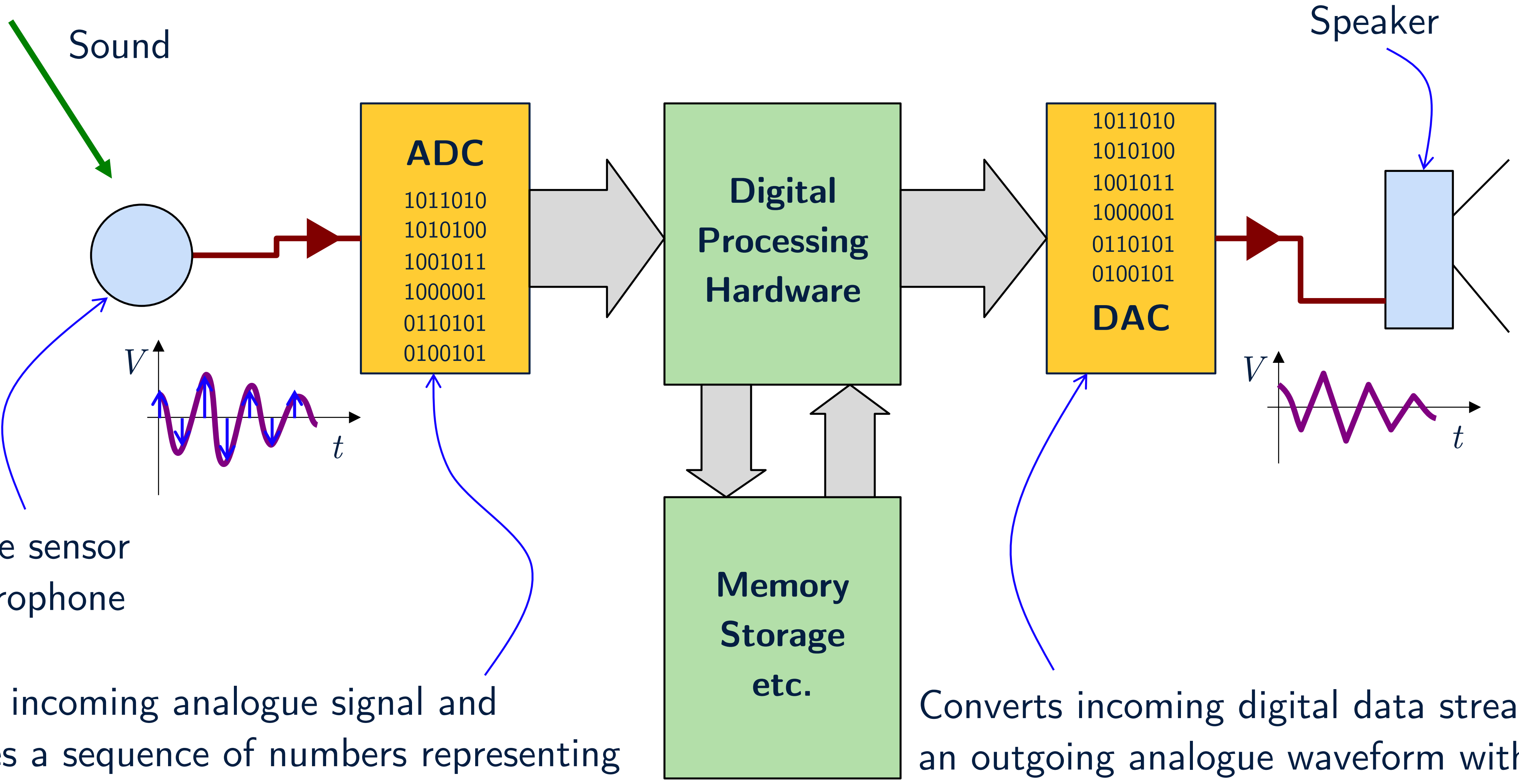
Data converters

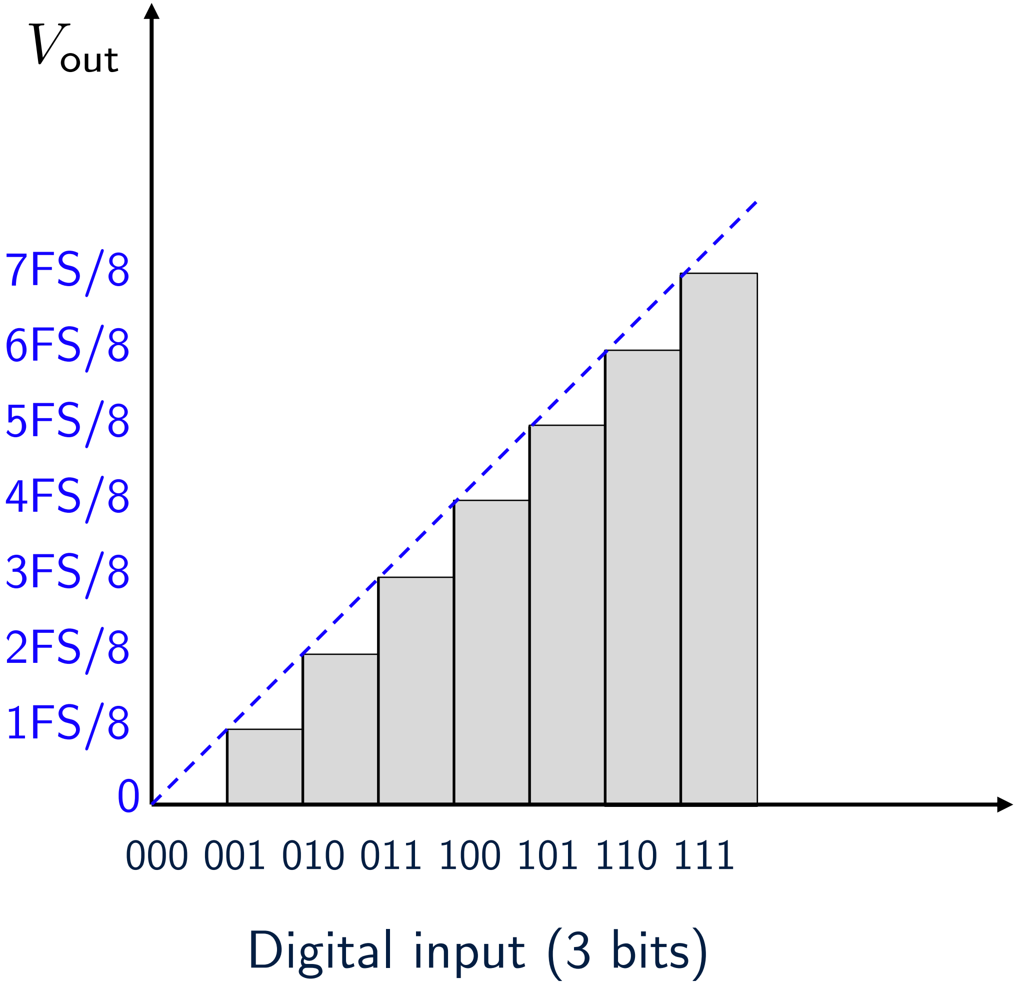


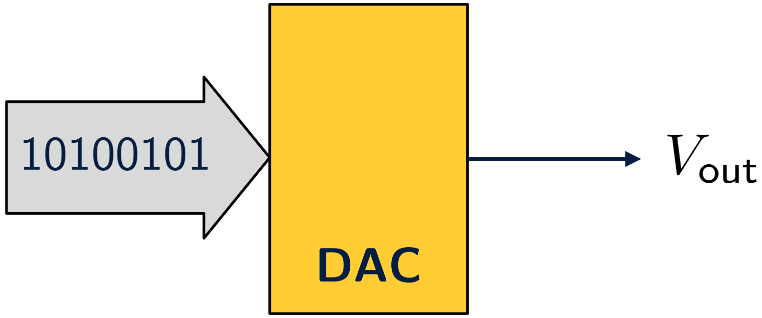
Analogue sensor
e.g. microphone

Samples incoming analogue signal and generates a sequence of numbers representing the signal amplitude at points in time

Converts incoming digital data stream into an outgoing analogue waveform with amplitude given by the stream of numbers

Digital-to-analogue converter (DAC) specification



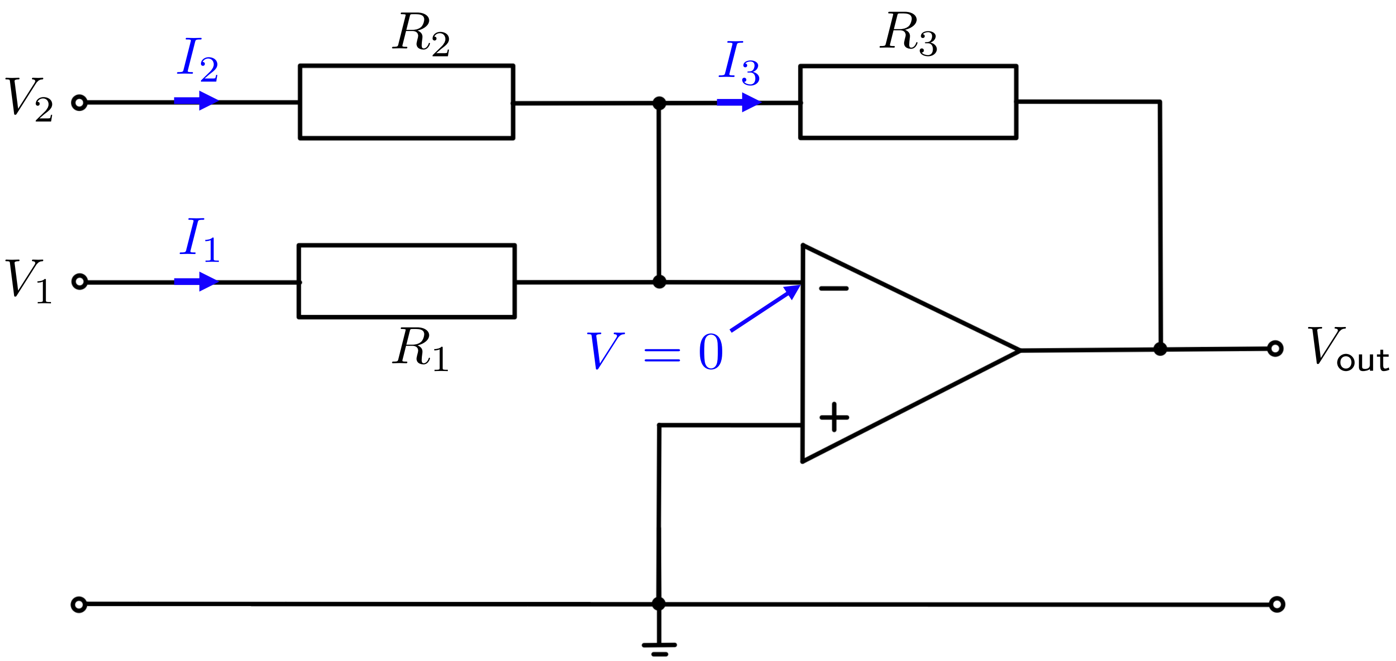


DAC is specified by:

1. the number of bits in the input **word**
2. the **full-scale** (FS) or maximum output voltage

It usually provides a linear relationship between the input binary sequence and the analogue voltage output

DAC architecture



$$V_{\text{out}} = -R_3\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$

Suppose we have a two-bit input, represented by V_1 and V_2

Set $R_3 = R_2 = 2R_1$, then

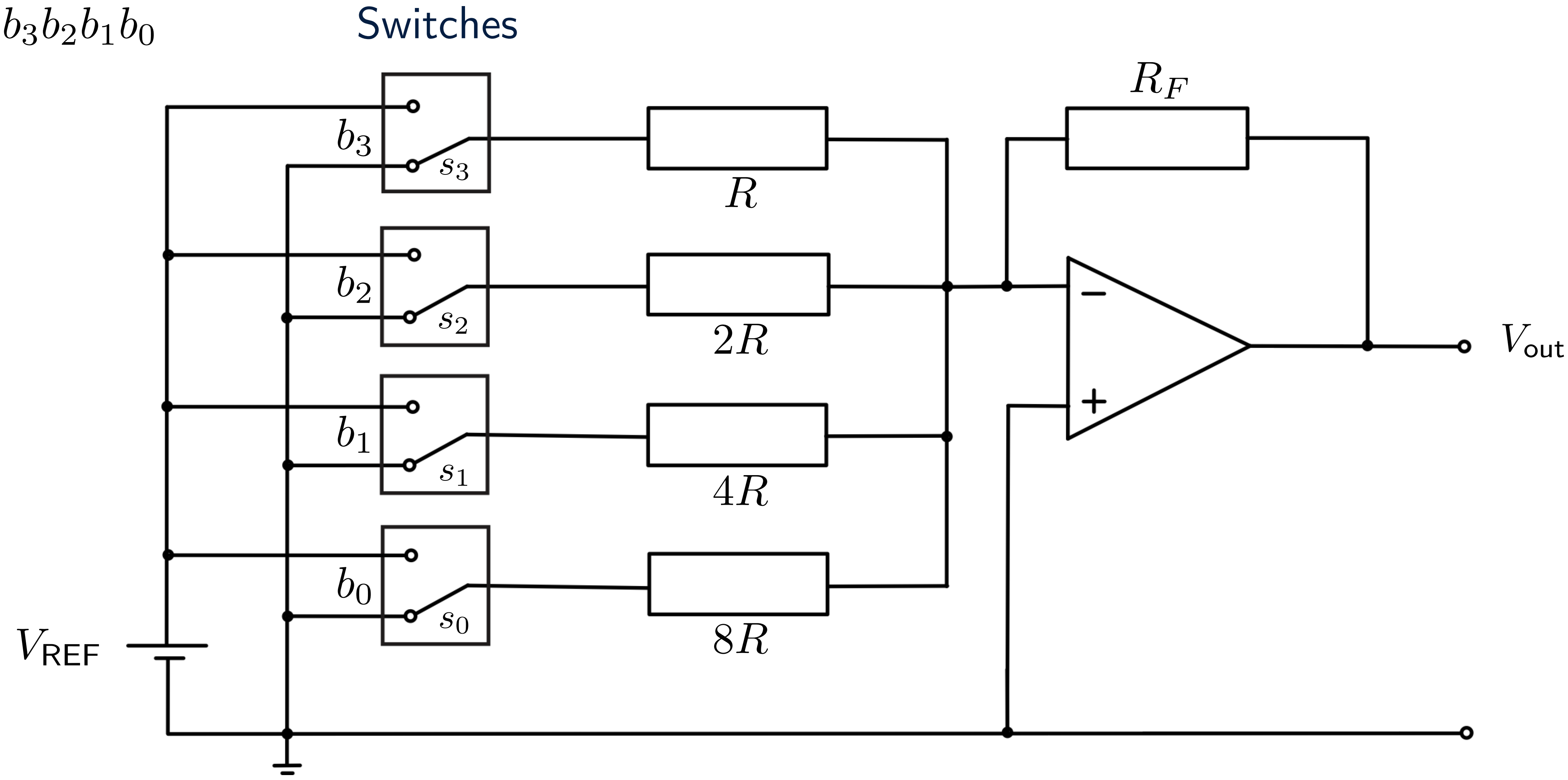
$$\boxed{V_{\text{out}} = -2V_1 - V_2}$$

V_2	V_1	V_{out}
0	0	-0 V
0	1	-1 V
1	0	-2 V
1	1	-3 V

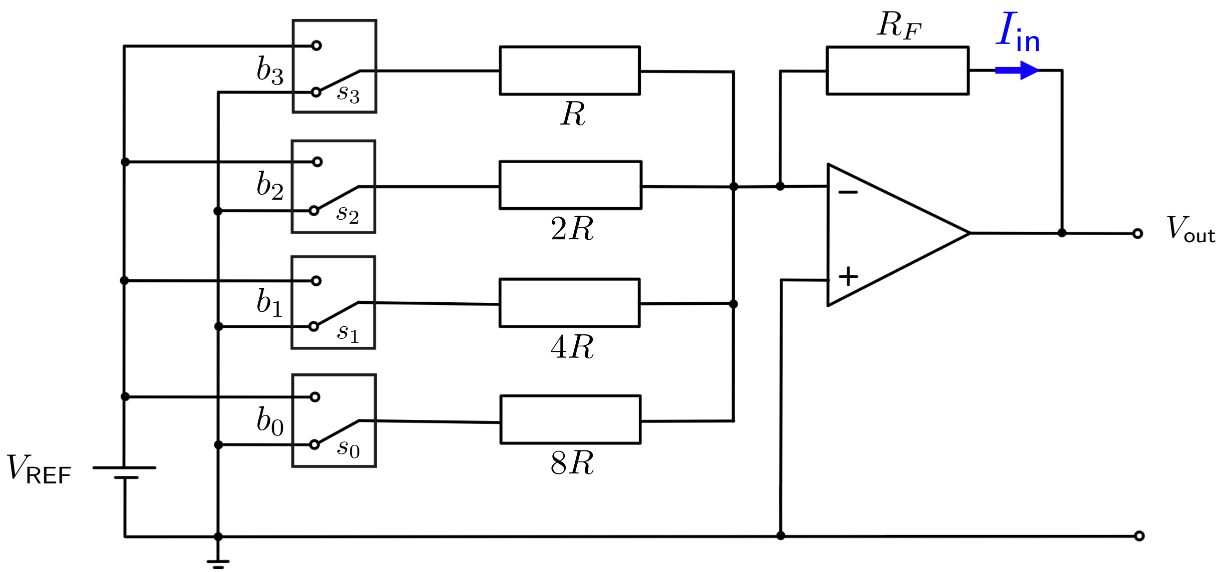
Terminal voltages

DAC architecture: 4-bit ladder

Input: $b_3 b_2 b_1 b_0$



4-bit DAC operation



Current into the feedback loop:

$$I_{\text{in}} = V_{\text{REF}} \left(\frac{b_3}{R} + \frac{b_2}{2R} + \frac{b_1}{4R} + \frac{b_0}{8R} \right)$$

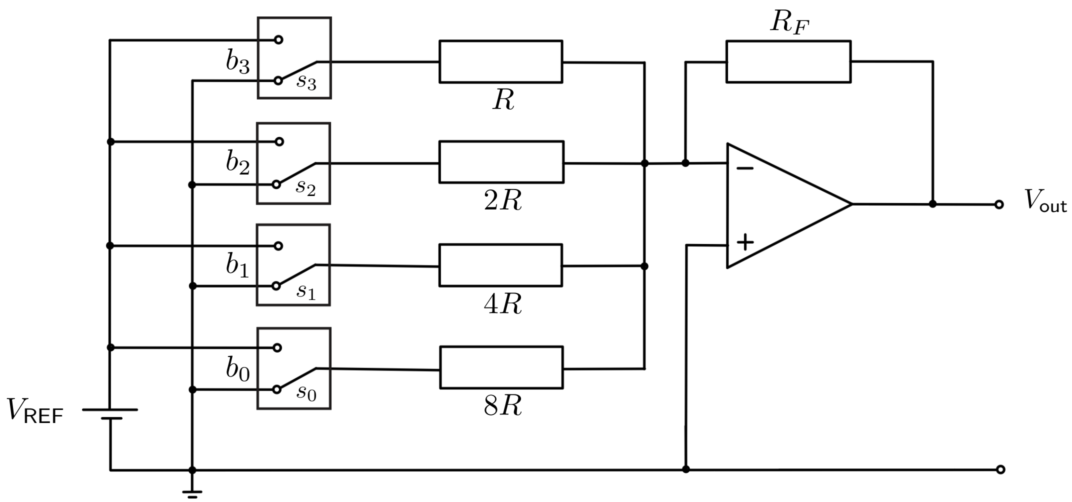
Voltage at output:

$$\boxed{V_{\text{out}} = -\frac{R_F}{R} V_{\text{REF}} \left(b_3 + \frac{b_2}{2} + \frac{b_1}{4} + \frac{b_0}{8} \right)}$$

Set $R = 2R_F$:

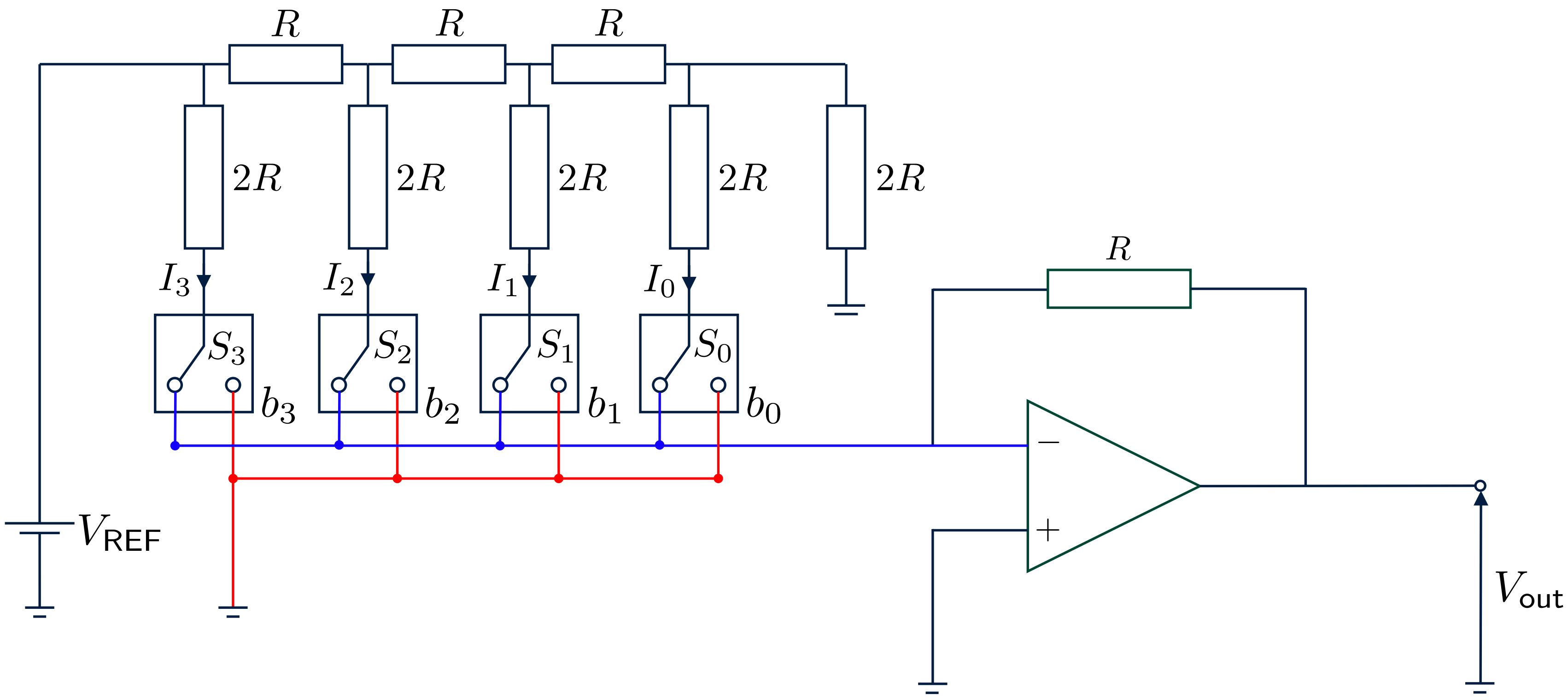
$b_3 b_2 b_1 b_0$	$V_{\text{out}}/V_{\text{REF}}$
0000	0
0001	$-1/16$
0010	$-2/16$
0011	$-3/16$
0100	$-4/16$
0101	$-5/16$
0110	$-6/16$
0111	$-7/16$
1000	$-8/16$
1001	$-9/16$
1010	$-10/16$
1011	$-11/16$
1100	$-12/16$
1101	$-13/16$
1110	$-14/16$
1111	$-15/16$

4-bit DAC limitations



- ▷ Needs an accurate constant reference voltage V_{REF}
  - $\Rightarrow$ must be low-noise to get low-noise output
- ▷ Variable current is drawn from the source
  - $\Rightarrow$ must have zero or near-zero output resistance
- ▷ Resistor values must be accurate to get correct scaling
  - $\Rightarrow$ e.g. with 12 bits, MSB $= 2^{11} = 2048$ so $\max R / \min R = 2048$, which is a big range to achieve accurately on an integrated circuit

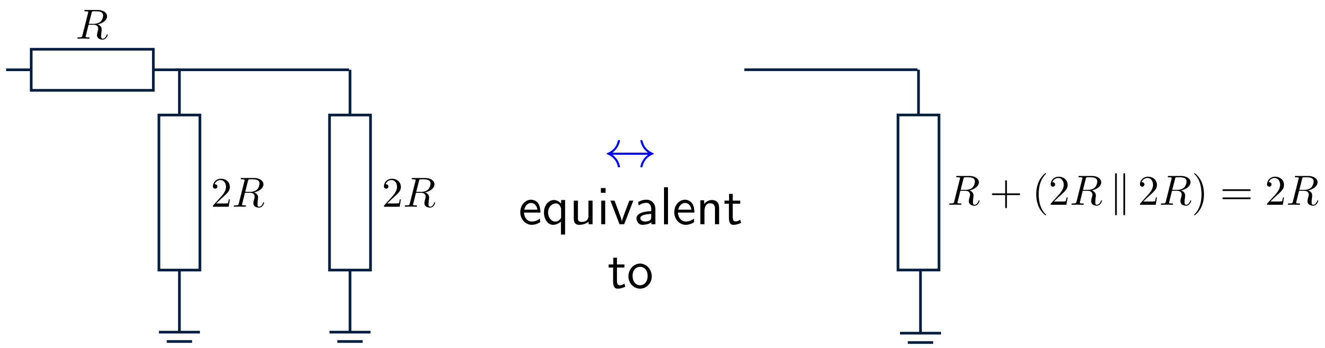
Improved ladder circuit: the R-2R ladder



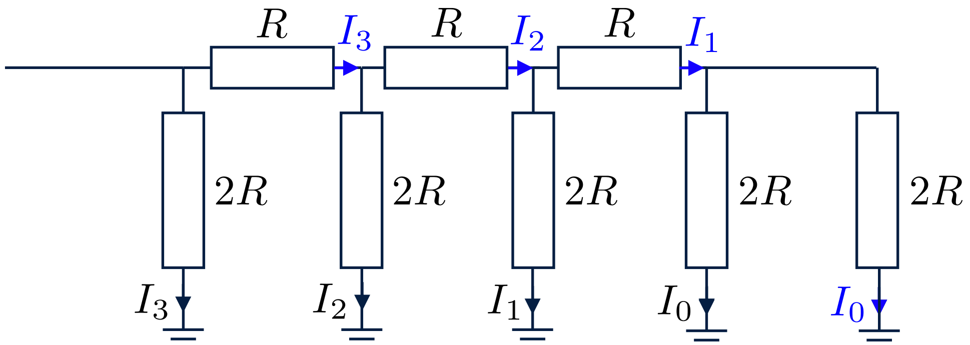
Binary input $b_3b_2b_1b_0$

R-2R ladder analysis

Each switch S_i is connected either to earth or to the virtual earth of the op-amp



$\leftrightarrow$
equivalent
to



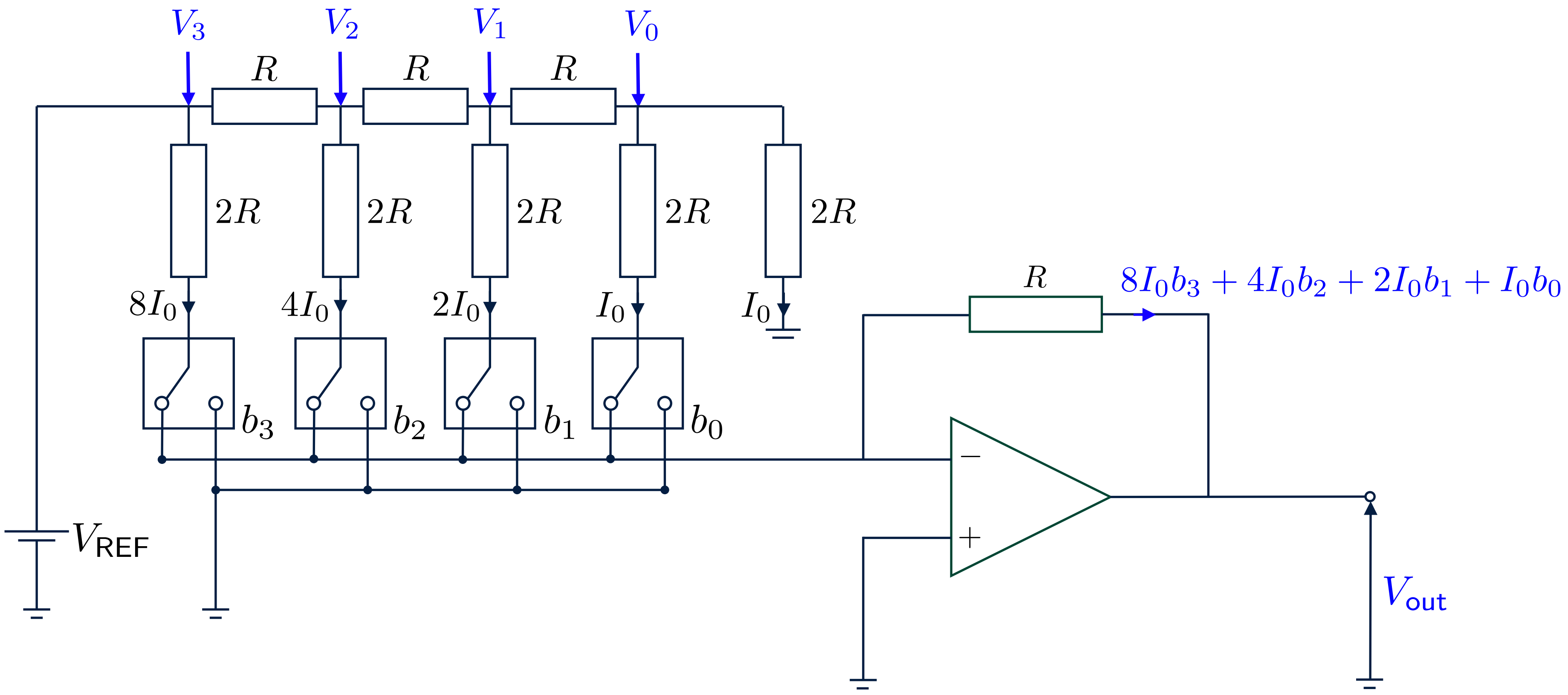
$\Rightarrow$

$$
\begin{aligned}
I_1 &= 2I_0 \\
I_2 &= 2I_1 \\
I_3 &= 2I_2
\end{aligned}
$$

Start at right-hand of ladder and work left

$$\boxed{I_3 = 2I_2 = 4I_1 = 8I_0}$$

R-2R ladder analysis



$$V_0 = 2I_0R$$

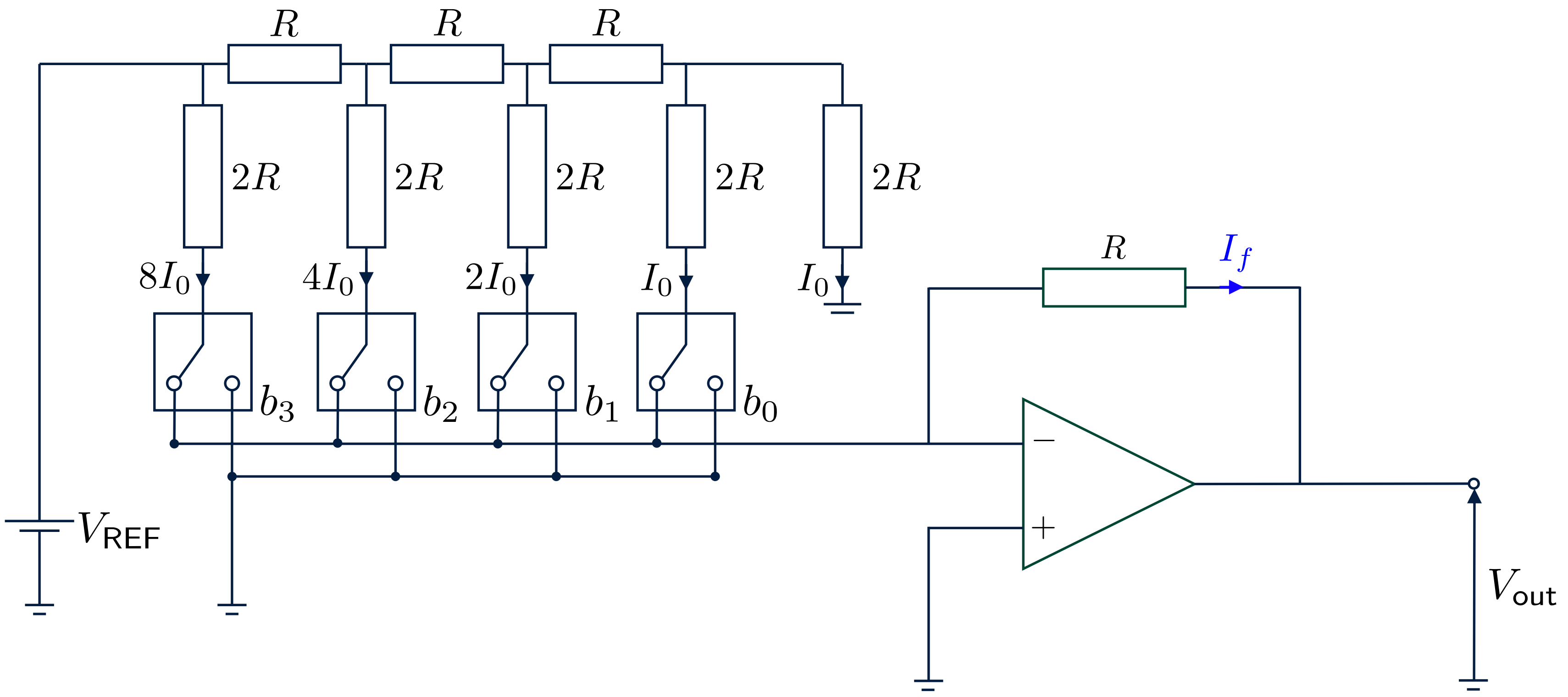
$$V_1 = 4I_0R, \quad V_2 = 8I_0R, \quad V_3 = 16I_0R = V_{\mathsf{REF}}$$

$$\Rightarrow \quad I_0 = V_{\mathsf{REF}}/16R$$

$$V_{\mathsf{out}} = -I_0R(8b_3 + 4b_2 + 2b_1 + b_0)$$

$$\Rightarrow \boxed{V_{\mathsf{out}} = -\frac{V_{\mathsf{REF}}}{16}(8b_3 + 4b_2 + 2b_1 + b_0)}$$

R-2R ladder analysis

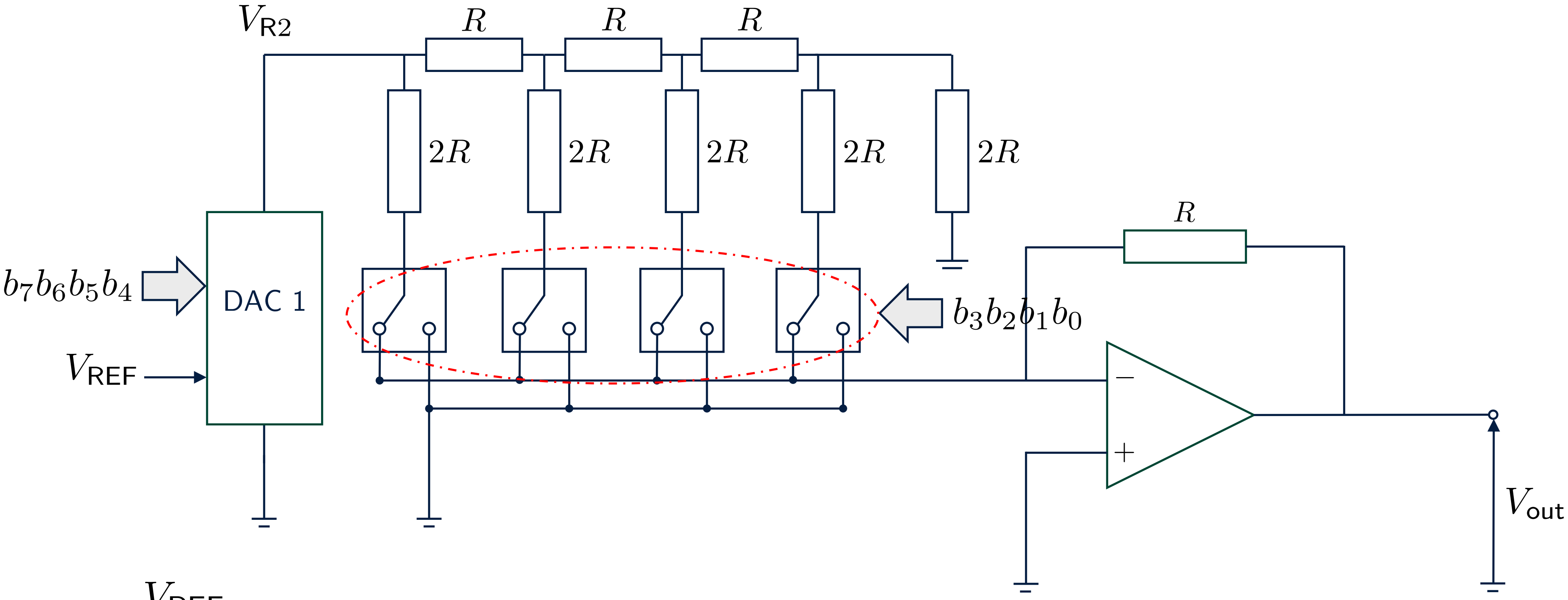


Example: $b_3 b_2 b_1 b_0 = 1010$

$$I_f = 8I_0 + 2I_0 = 10I_0$$

$$\Rightarrow \quad V_{\text{out}} = -\frac{10}{16} V_{\text{REF}}$$

Multiplying DAC (MDAC)



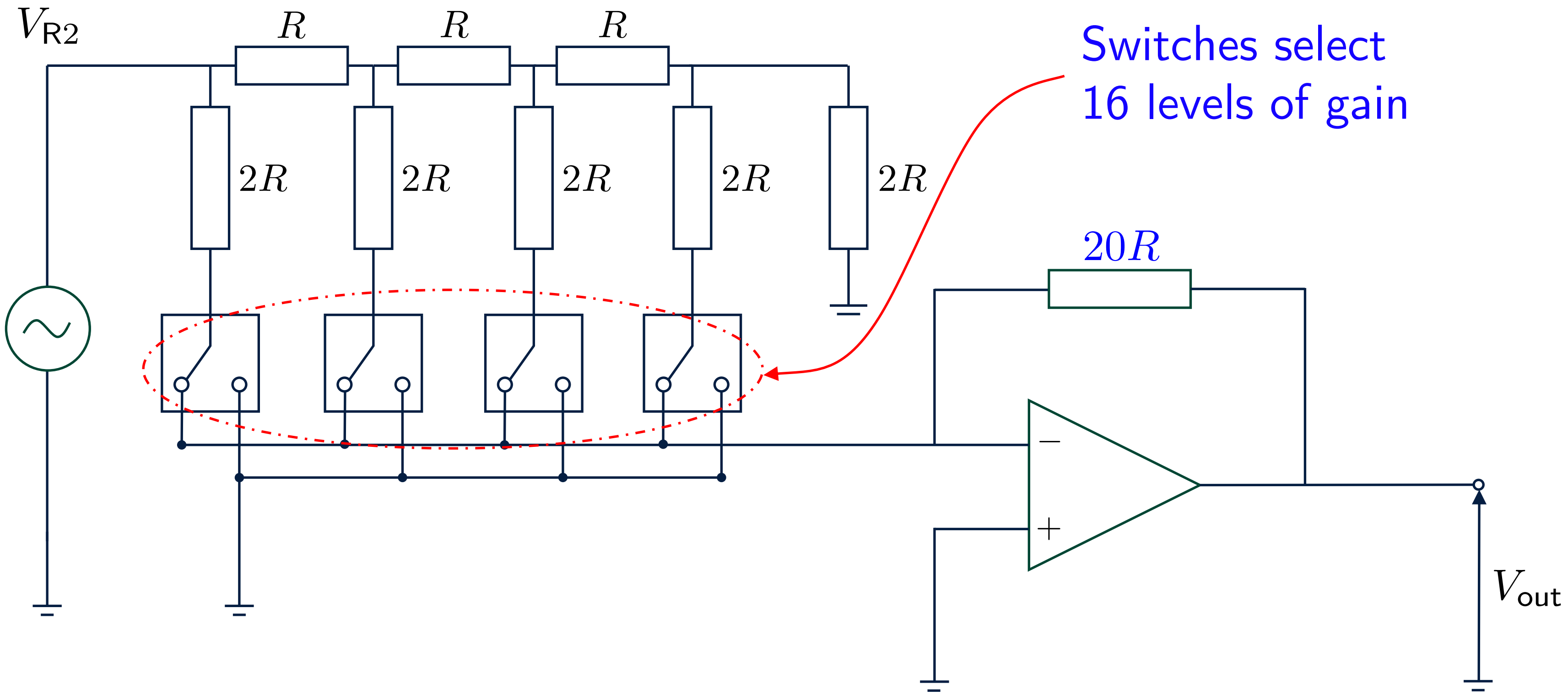
$$V_{\mathrm{R2}} = -\frac{V_{\mathrm{REF}}}{16}(8b_7 + 4b_6 + 2b_5 + b_4)$$

$$V_{\mathrm{out}} = -\frac{V_{\mathrm{R2}}}{16}(8b_3 + 4b_2 + 2b_1 + b_0)$$

$$\Rightarrow \quad V_{\mathrm{out}} = \frac{V_{\mathrm{REF}}}{256}(8b_7 + 4b_6 + 2b_5 + b_4)(8b_3 + 4b_2 + 2b_1 + b_0)$$

Output voltage proportional to the product of the numbers represented by the two binary inputs

DAC as a variable gain amplifier



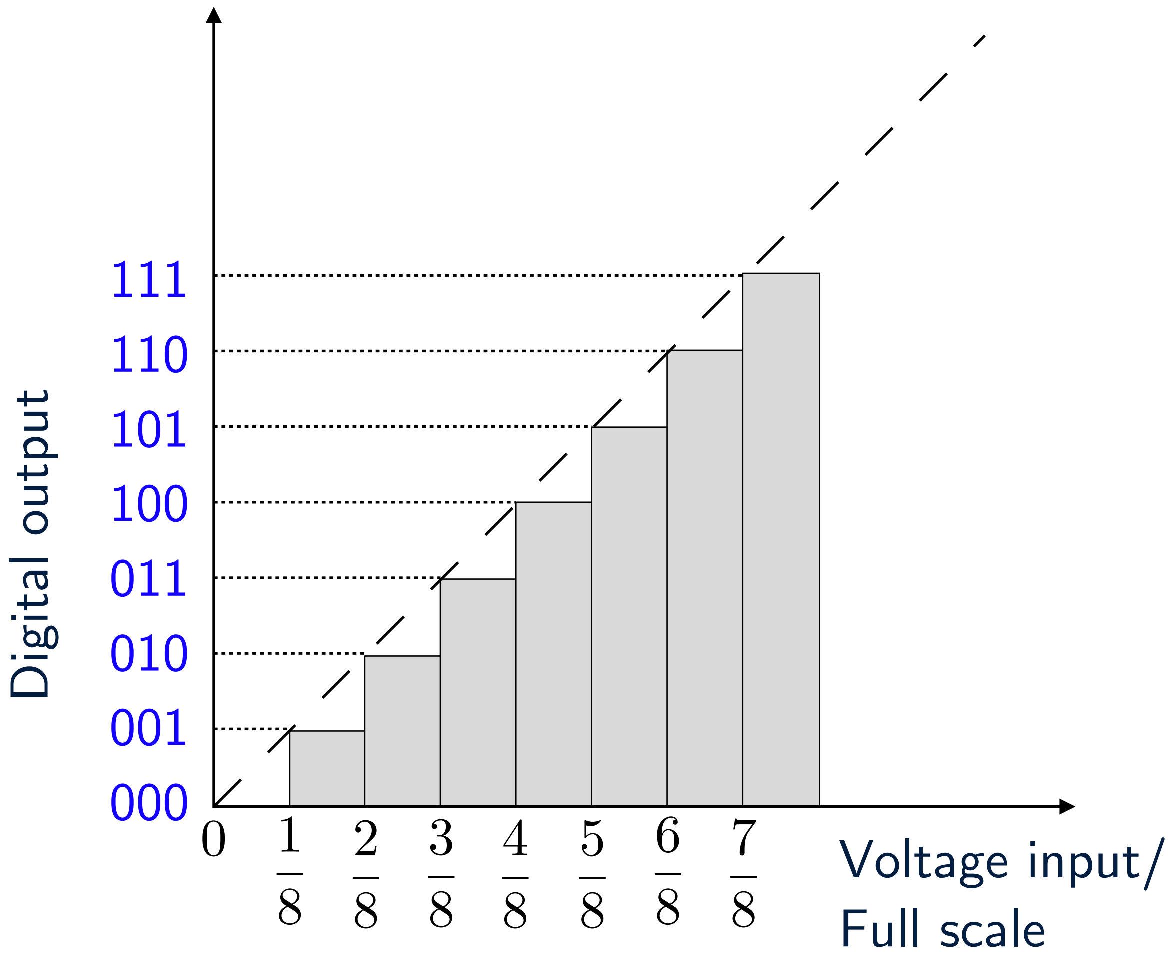
Signal to be amplified: V_{in}

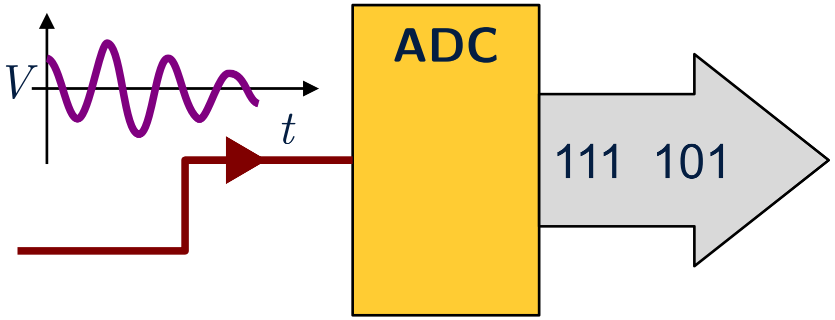
Switches select 16 levels of gain

$$V_{\text{out}} = -\frac{20}{16}(8b_3 + 4b_2 + 2b_1 + b_0)V_{\text{in}}$$

Analogue-to-digital converter (ADC)

Generates a binary number with value proportional (within rounding error) to applied input voltage





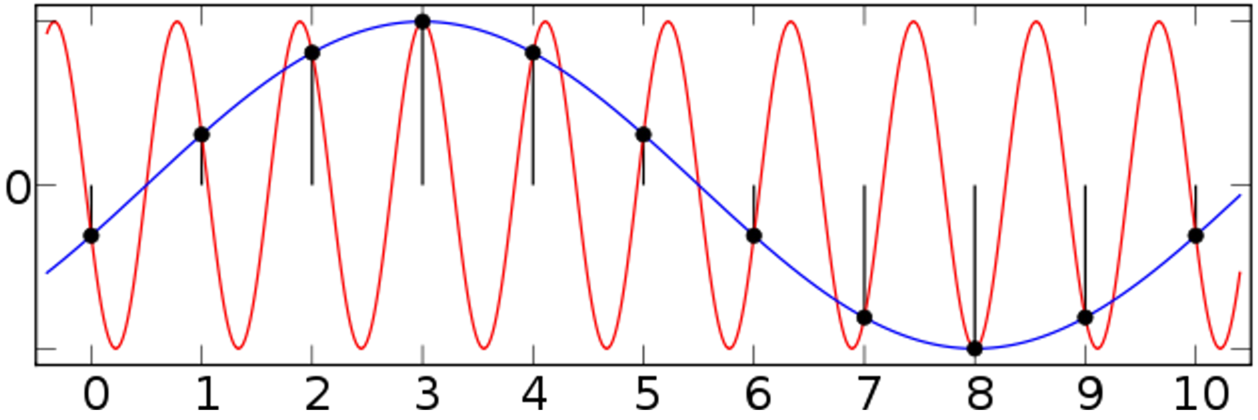
- ⋆ Output is quantised
- ⋆ Rounding error up to $\pm\frac{1}{2}$ LSB
- ⋆ Best performance if max input $\approx$ full scale

ADC Limitations

- ▷ Output voltage V_{LSB} corresponding to LSB depends on number of bits: $V_{\mathsf{LSB}} = \dfrac{V_{\mathsf{FS}}}{2^n}$

  e.g. if full-scale $V_{\mathsf{FS}} = 1\,\mathsf{V}$ and $n = 12\,\mathsf{bits}$, then $V_{\mathsf{LSB}} = \dfrac{1}{4096} = 0.244\,\mathsf{mV}$

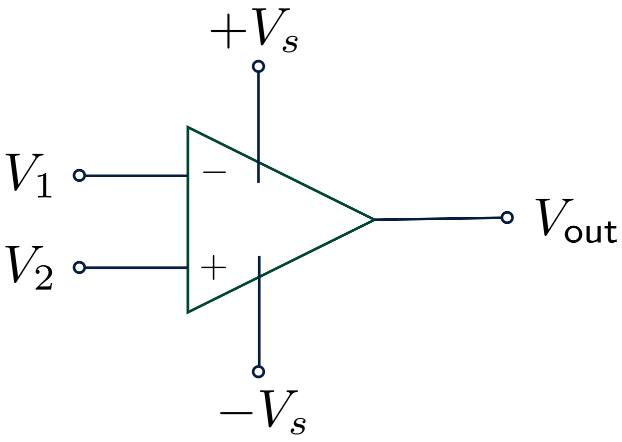
- ▷ Using more bits reduces quantisation error $= \pm\frac{1}{2}V_{\mathsf{LSB}}$ but requires more time to do a conversion
- ▷ To maximize range of input signal, we usually need to amplify the signal before input to ADC
- ▷ To avoid aliasing, we usually need to low-pass filter the signal before input to ADC



Types of ADC

- Parallel (flash) converters
  - Fast conversion
  - Expensive for large n
- Successive-approximation converters
  - Slower, simpler, and cheaper

Parallel (flash) ADC: comparator

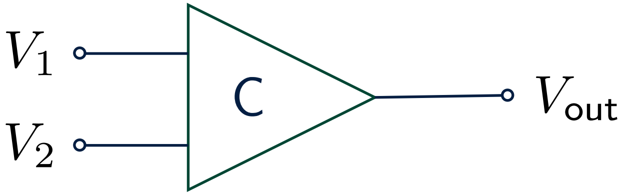


If $|V_2 - V_1|$ is small enough, then

$$V_{\text{out}} = A_{\text{OL}}(V_+ - V_-) = A_{\text{OL}}(V_2 - V_1)$$

But the op amp has no feedback, so $A_{\text{OL}} \gg 1$, and in practice we get:

$$V_{\text{out}} = \begin{cases} +V_s & \text{if } V_2 > V_1 \\ -V_s & \text{otherwise} \end{cases}$$

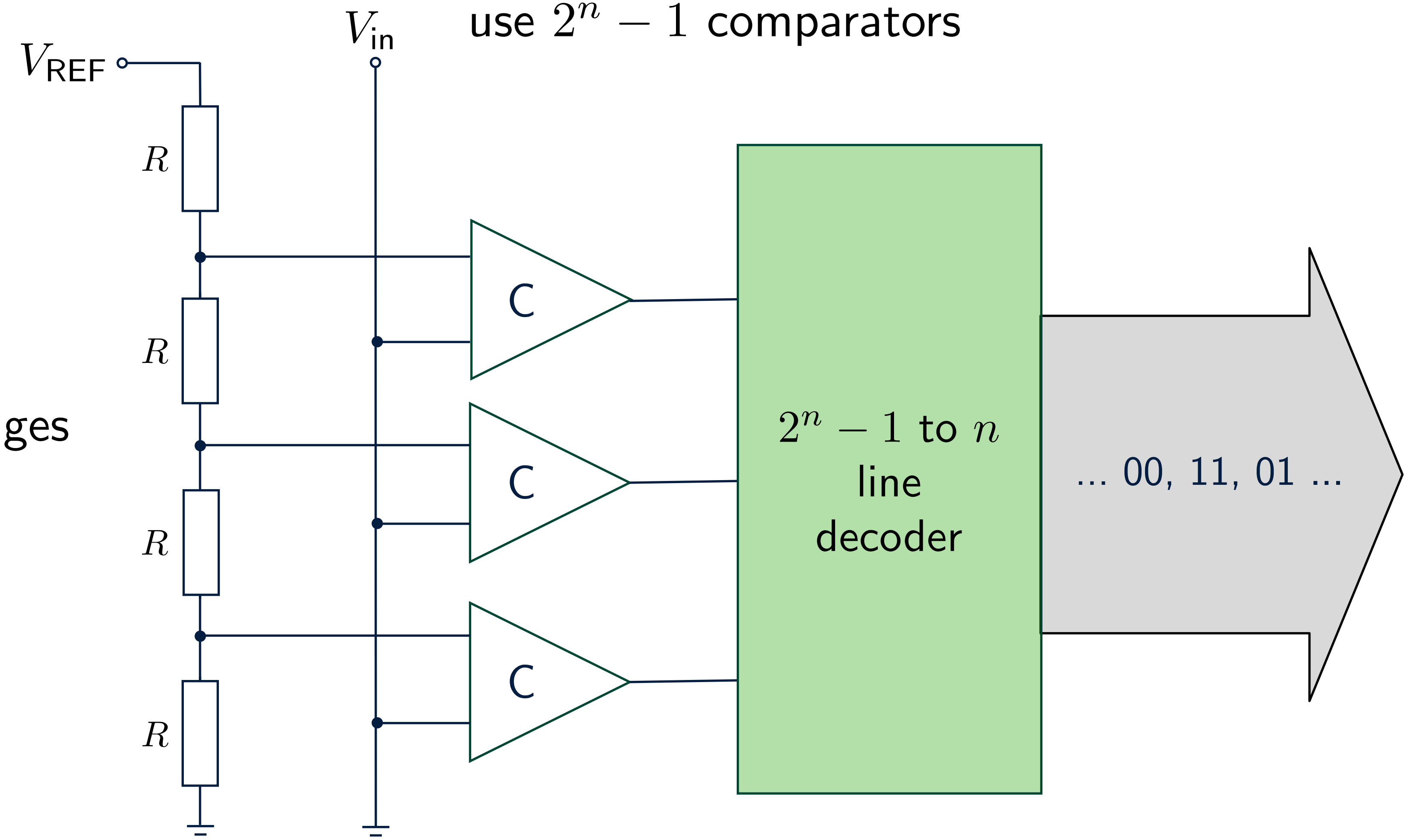


Simplified comparator symbol

Parallel (flash) ADC

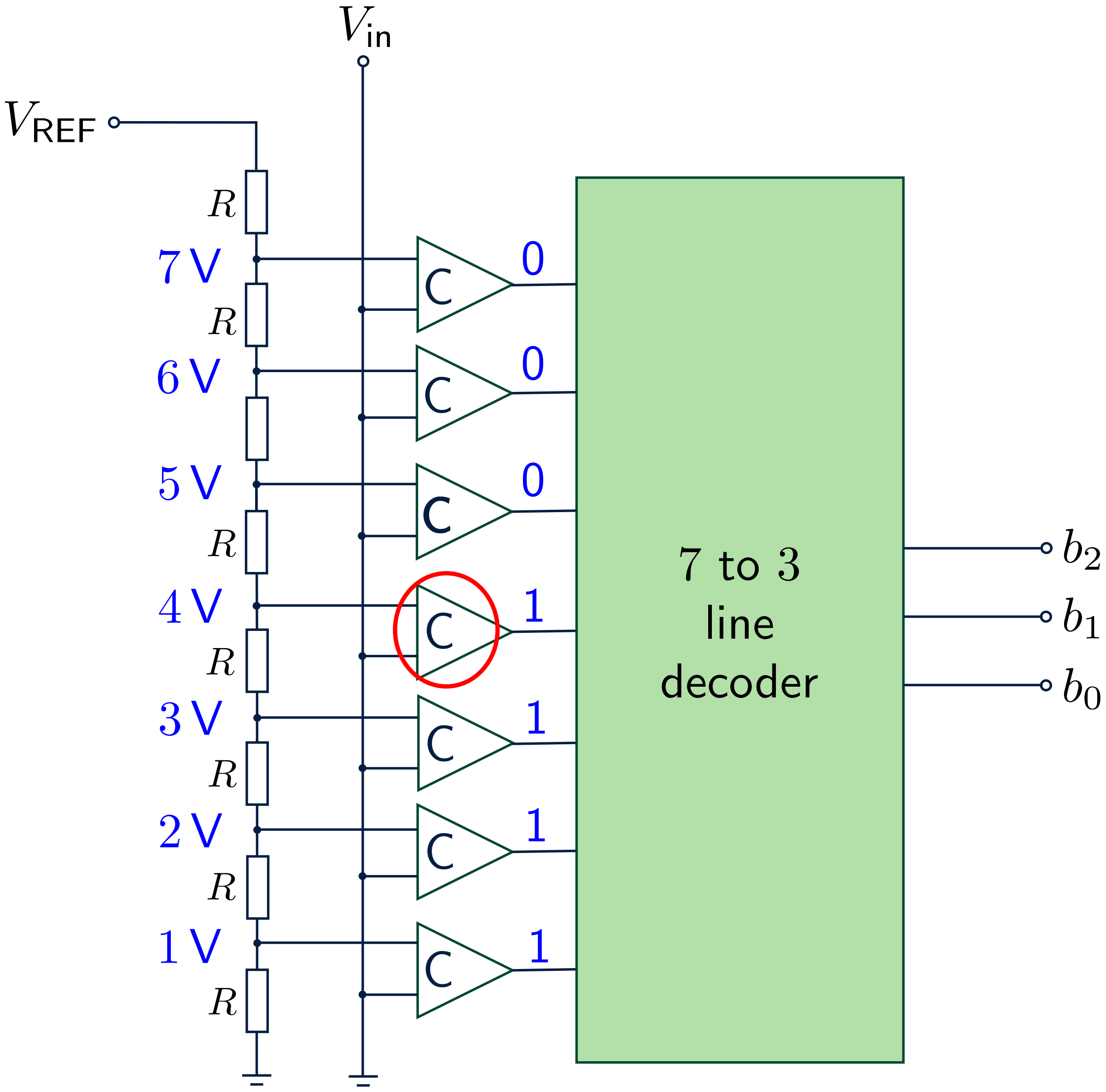
For an n-bit flash ADC,
use $2^n - 1$ comparators

2^n resistors generate
$2^n - 1$ reference voltages
to compare with V_{in}



Parallel (flash) ADC

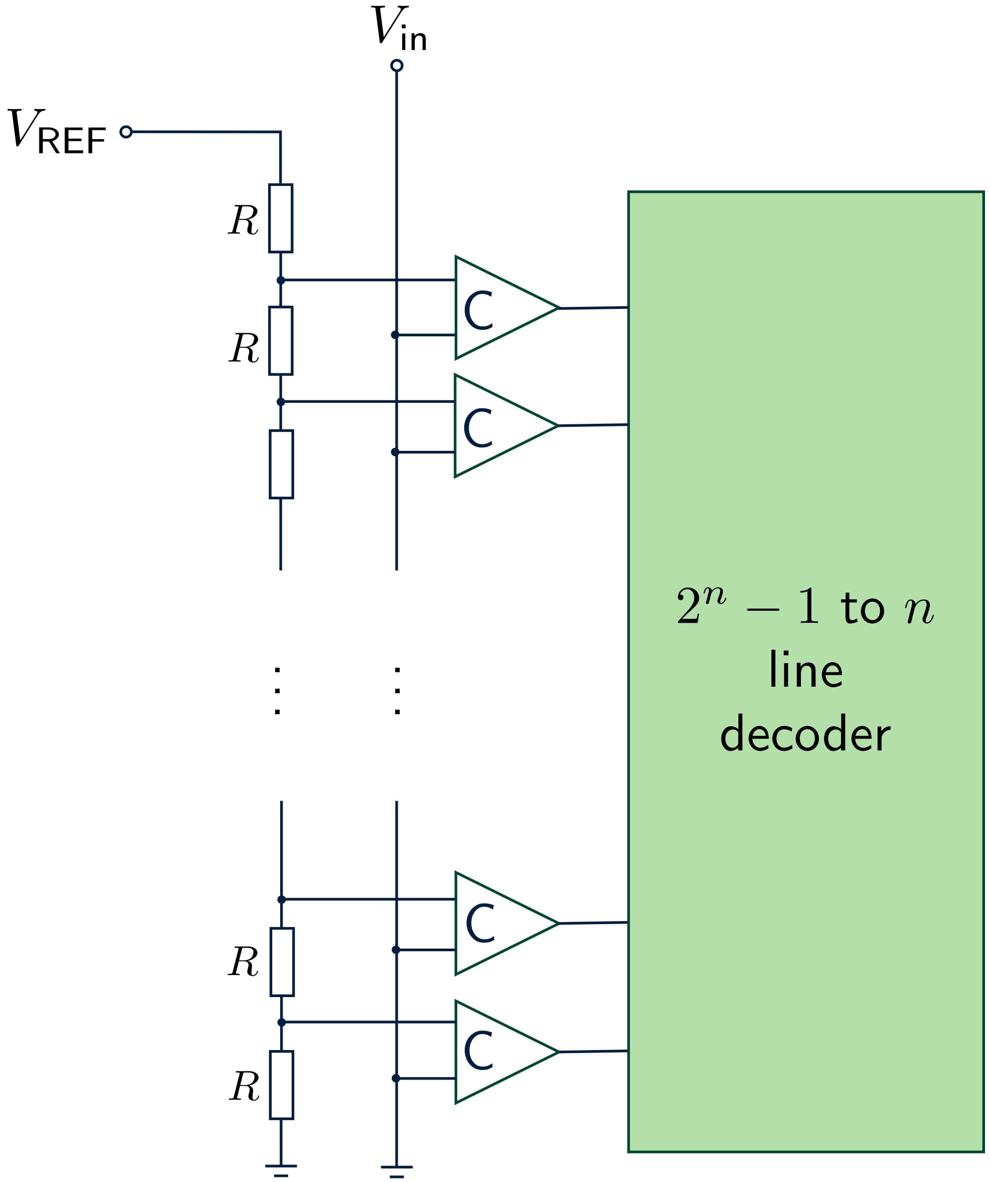
e.g. $n = 3$:



If $V_{\text{REF}} = 8\,\text{V}$, then $V_{\text{in}} = 4.5\,\text{V}$ gives:

$$b_2 = 1$$
$$b_1 = 0 \quad \Rightarrow \quad b_2 b_1 b_0 = 100 = 4_{10}$$
$$b_0 = 0$$

Parallel (flash) ADC



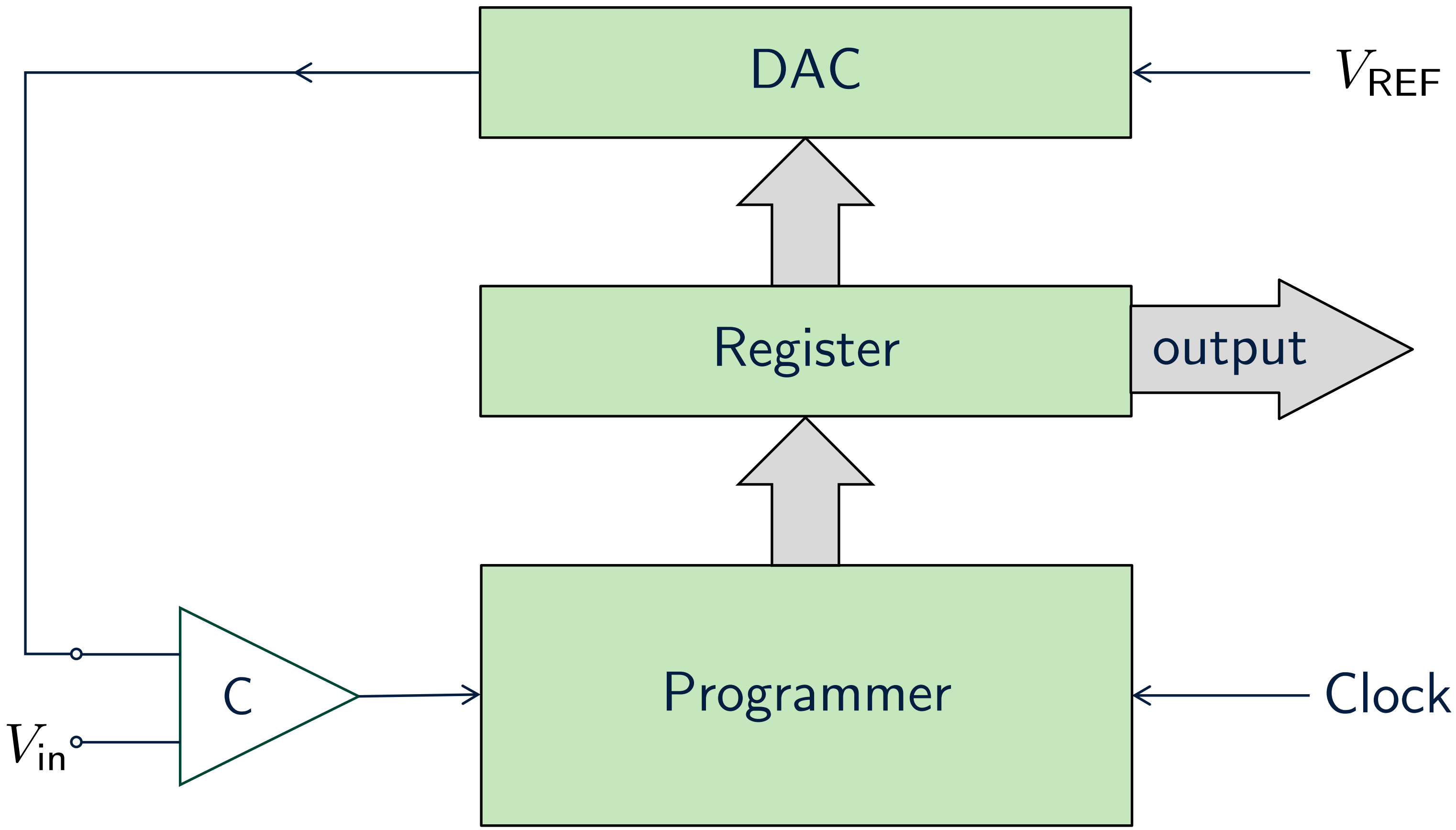
Fast: very little time required for conversion

Requires lots of components (for large number of bits, higher power consumption and bigger size)

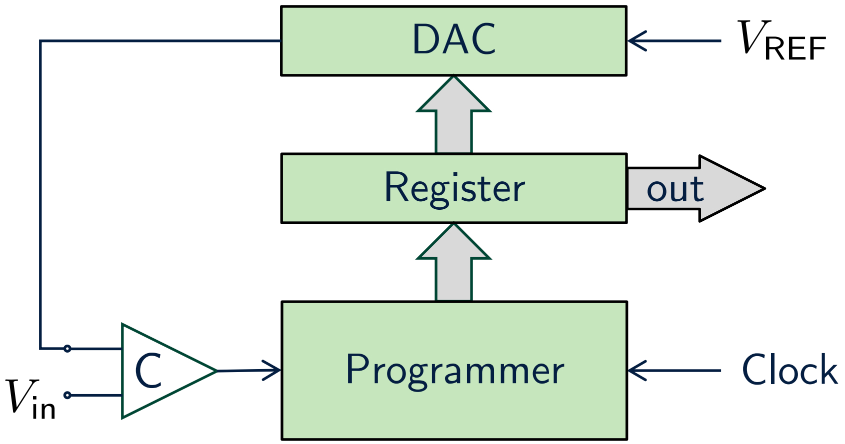
Integrated circuits use lots of silicon for so many resistors and transistors

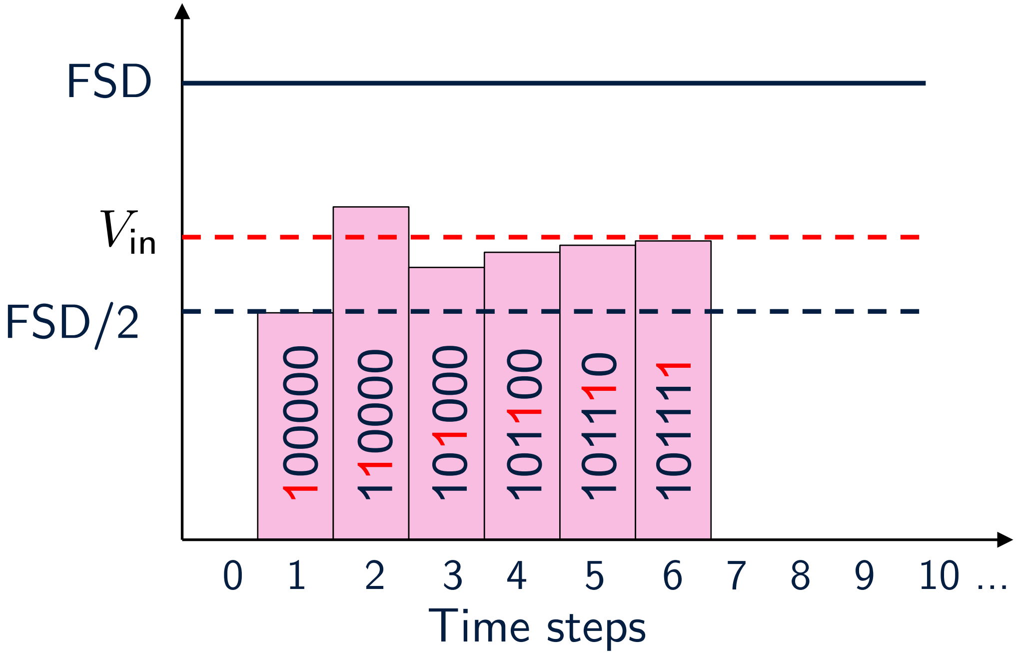
Expensive: ADCs with high order (large numbers of bits) require very small voltage differences between levels – noise and precision of components are problematic

Successive approximation ADCs (SAADCs)



SAADC





- Works by comparing input signal to test voltage
- Test voltage is generated by DAC (e.g. 6-bit DAC):

$$V_{\text{REF}}\left(\frac{b_0}{64}+\frac{b_1}{32}+\frac{b_2}{16}+\frac{b_3}{8}+\frac{b_4}{4}+\frac{b_5}{2}\right)$$

- Programmer runs a simple algorithm:

  If test voltage $>$ input, reduce test voltage
  If test voltage $<$ input, increase test voltage
  Repeat until all bits set

- Only needs 1 comparator
  No matching of resistors required

- Needs digital circuits to store values and run programmer

- Conversion takes n cycles to completely define all bits.

- Input signal needs to remain stable for this time and not change by more than 0.5 x LSB

Frequency limitation

Assume the input signal is sinusoidal:

$$V_{\text{in}} = V_a \sin(2\pi f t) = \frac{1}{2} V_{\text{REF}} \sin(2\pi f t)$$

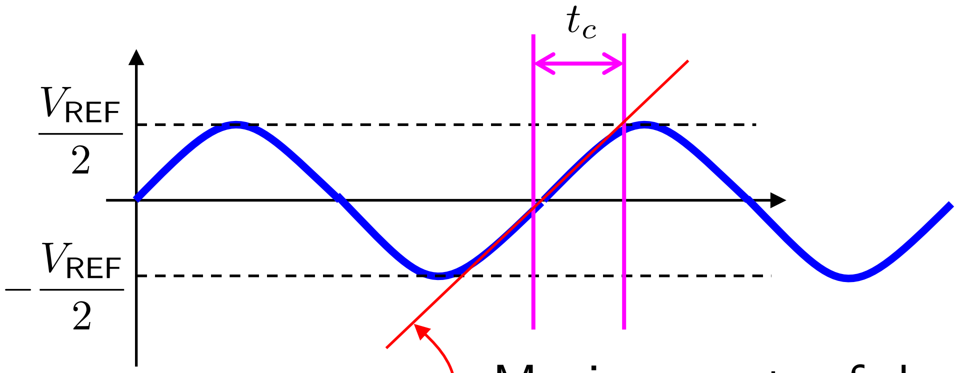
Assume peak-to-peak amplitude is V_{REF}

Maximum allowable variation in input signal is $\frac{1}{2}$ LSB:

$$\Delta V_{\text{in}}^{\max} = \frac{1}{2} \frac{V_{\text{REF}}}{2^n}$$

Rate of change of input:

$$\frac{dV_{\text{in}}}{dt} = \pi f V_{\text{REF}} \sin(2\pi f t)$$



Maximum rate of change:

$$\left|\frac{dV_{\text{in}}}{dt}\right| = \pi f V_{\text{REF}}$$

Approximate change in signal over conversion time t_c:

$$\left|\frac{dV_{\text{in}}}{dt}\right| t_c \le \frac{1}{2} \frac{V_{\text{REF}}}{2^n} \quad \Rightarrow \quad \pi f V_{\text{REF}} t_c \le \frac{V_{\text{REF}}}{2^{n+1}} \quad \Rightarrow \quad \boxed{f_{\max} = \frac{1}{\pi t_c 2^{n+1}}}$$

Frequency limitation example

- Assume
  - ⋆ 8-bit ADC ($n = 8$)
  - ⋆ total time required for conversion is $10\,\mu$s ($t_c = 10^{-5}$)

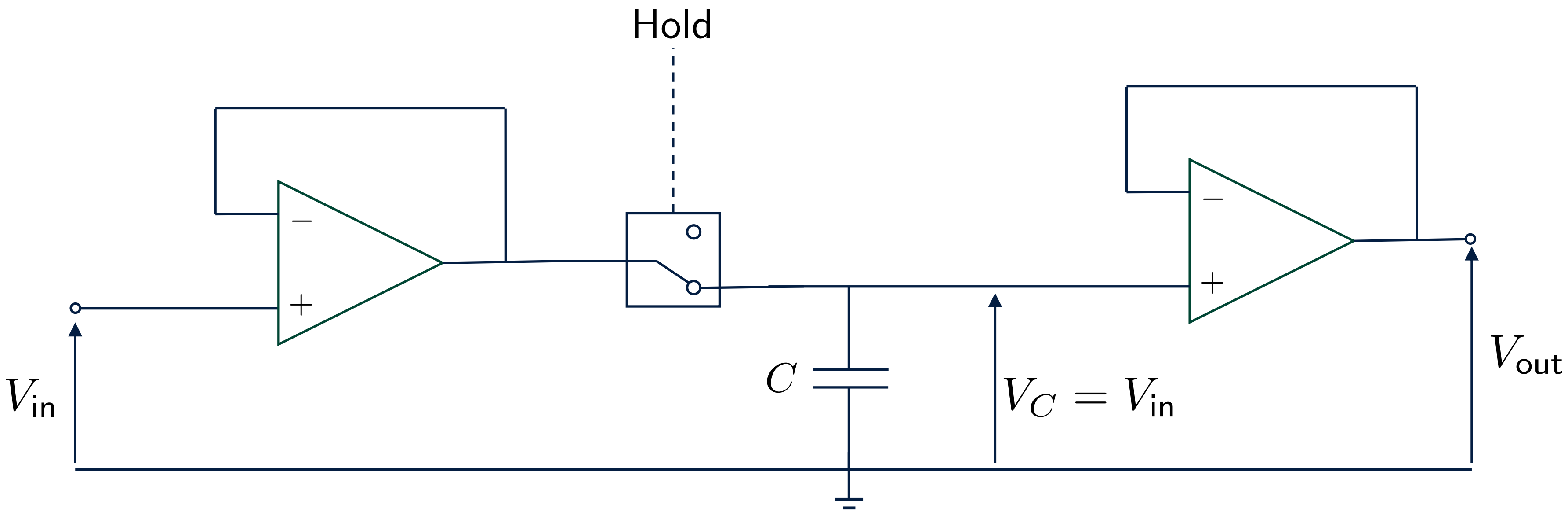
  then

  $$f_{\max} = \frac{1}{\pi t_c 2^{n+1}} = \frac{1}{\pi \times 10^{-5} \times 2^9} = 62\,\text{Hz}$$

  This is very slow ⇒ applications are limited

- A better alternative is to prevent the input changing during the acquisition process

Sample and hold



Closing the switch charges the capacitor C

The capacitor is charged during time t_a (the **aperture time**): small C implies it charges rapidly

The switch is opened and a second follower op amp supplies the voltage $V_{\text{out}} = V_C$ to input to ADC

$$\boxed{f_{\max} = \frac{1}{\pi t_a 2^{n+1}}} \longleftarrow \text{choose } C \text{ so that } t_a \ll t_c$$

Summary

- DACs based on op amp summing amplifiers
- ADCs based on op amp comparators (in parallel or in time sequence)
- Rely on sampling – aliasing needs to be considered
- Speed limitations to due conversion time – improved with sample and hold
- Resolution limits (size of LSB)

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